

What is claimed is:

1. A semiconductor device comprising:
 - a capacitor having a bottom electrode, a dielectric layer and an upper electrode, formed on a semiconductor substrate;
 - a first insulating layer formed on the semiconductor substrate to cover the capacitor;
 - a first contact plug formed in a first via hole of the first insulating layer and electrically connected to the bottom and upper electrodes;
 - a first metal wiring formed on the first insulating layer and connected to the bottom electrode through the first contact plug;
 - a second contact plug formed on the first insulating layer and connected to the upper electrode through the first contact plug;
 - a second insulating layer formed on the first insulating layer to cover the first metal wiring and the second contact plug;
 - an anti-fuse formed in a certain thickness in a second via hole of the second insulating layer and electrically connected to the second contact plug;
 - a third contact plug filling the second via hole on the anti-fuse; and
 - a second metal wiring formed on the second insulating layer and electrically connected to the third contact plug.

2. The semiconductor device of claim 1, wherein the first and second metal wirings are arranged perpendicular to each other.

3. A method of manufacturing a semiconductor device, comprising:

forming capacitors having a bottom electrode, a dielectric layer and an upper electrode on a semiconductor substrate;

forming a first insulating layer on the semiconductor substrate to cover the capacitors;

forming a plurality of first via holes exposing surfaces of the bottom and upper electrodes by selectively patterning the first insulating layer;

forming a plurality of first contact plugs by filling the first via holes with metal materials;

forming first metal wiring connected to the bottom electrodes through the first contact plugs and second contact plugs connected to the upper electrodes through the first contact plugs, on the first insulating layer;

forming a second insulating layer on the first insulating layer to cover the first metal wiring and the second contact plugs;

forming a plurality of second via holes exposing surfaces of the second contact plugs by selectively patterning the second insulating layer;

successively depositing the first and second metal layers on the second insulating layer including the second via holes;

forming anti-fuses and third contact plugs in the second via holes by planarizing the first and second metal layers with the second insulating layer; and

forming second metal wiring electrically connected to the anti-fuses and the third contact plugs, on the second insulating layer.